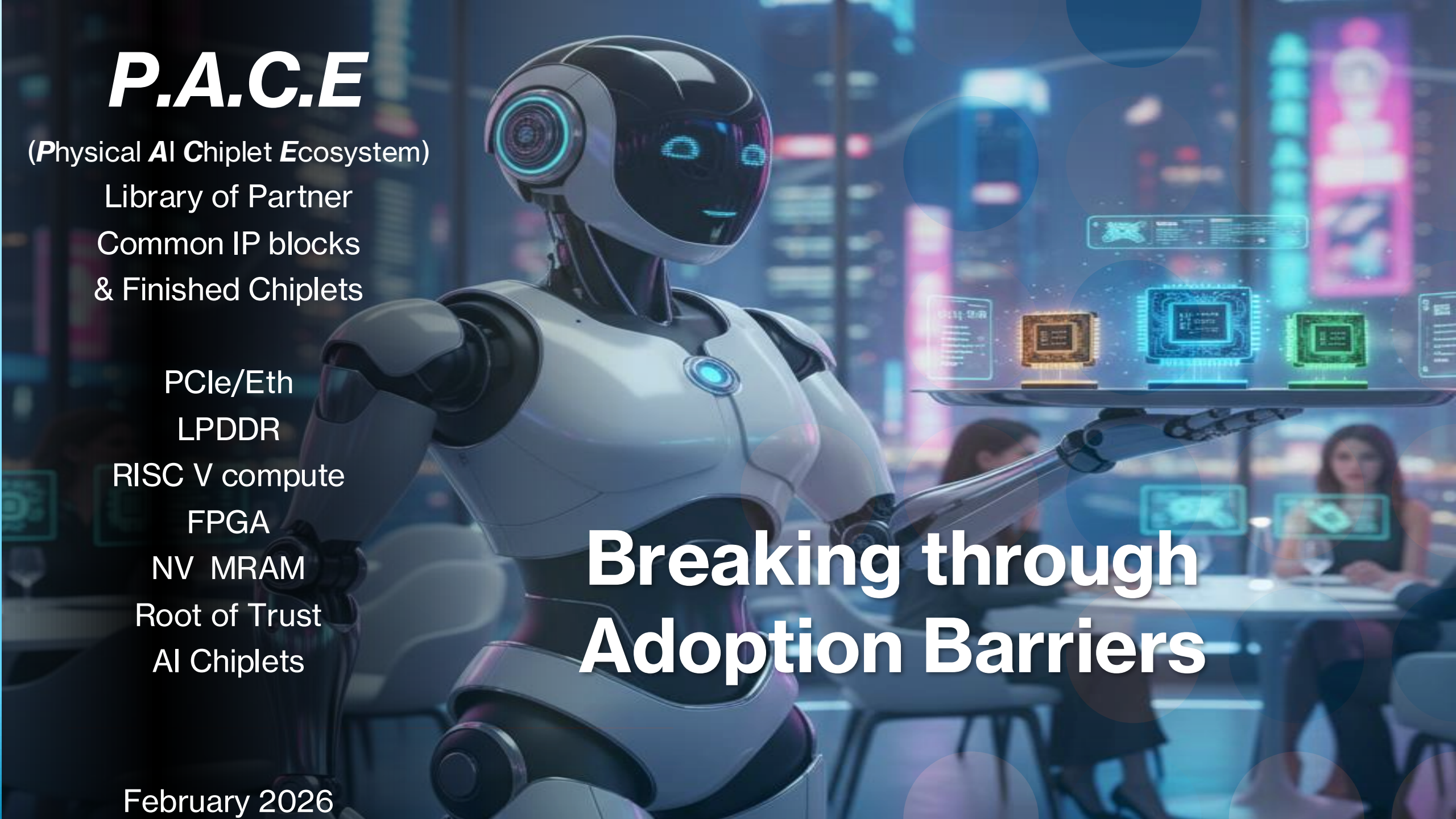
Breaking the Chiplet Walls

www.pacechiplets.com



P.A.C.E

(***P***hysical ***A***I ***C***hiplet ***E***cosystem)

Library of Partner
Common IP blocks
& Finished Chiplets

PCIe/Eth
LPDDR
RISC V compute
FPGA
NV MRAM
Root of Trust
AI Chiplets

Breaking through Adoption Barriers

February 2026

Zero Cost to USE PHY for MPW @ 28nm TSMC node

PHYSICAL AI

There is a better way

Total Solution for PHYSICAL AI & Open Chiplets

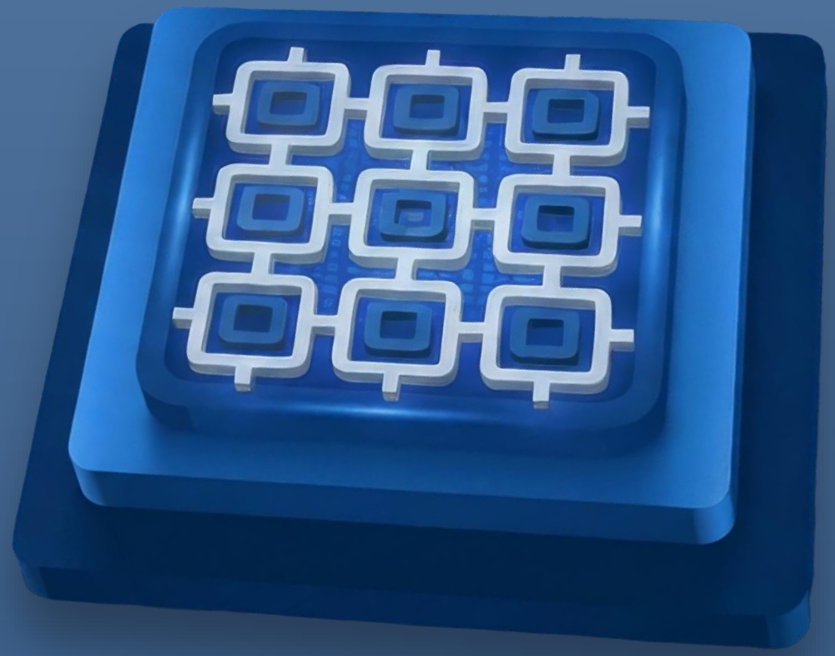
0.1 pj/bit 4X Lower Power	20X Lower Area cost	2X Lower Latency	2X Lower Dev Costs
75% Lower Power	**95% lower Area**	**< 50% Latency**	**< HALF Dev COST**

YorChip Patented PHY
Optimized for PHYSICAL AI / Edge
100% Digital PHY UCIe-3D, BoW.Flexi

P.A.C.E. Team

- Sofics – world leader in custom I/O – from 40nm to 2nm
- Dolphin Technology – Memory IP experts – from 2nm to 28nm DDR, LPDDR IP critical for AI
- Chip Interfaces – JESD204 IP experts for ADC/DAC interfacing, Interlaken and UCIe IP
- Blumind – Ultra Low Power AI solutions – award winning – Chiplets in future
- QuickLogic – world leader in eFPGA – sensor fusion, design flexibility – Chiplets in future
- Crypto Quantique – leader in IP for ROT and PUF and support for PQC
- Everspin – MRAM – leader in high-performance MRAM, suitable for AI, Chiplets in future
- GSOC – start up developing Chiplet platform, RISC V based compute, security and management
- YorChip – start up - patented best in class power and area PHY enabling PHYSICAL Chiplets

Co-Develop with System Users

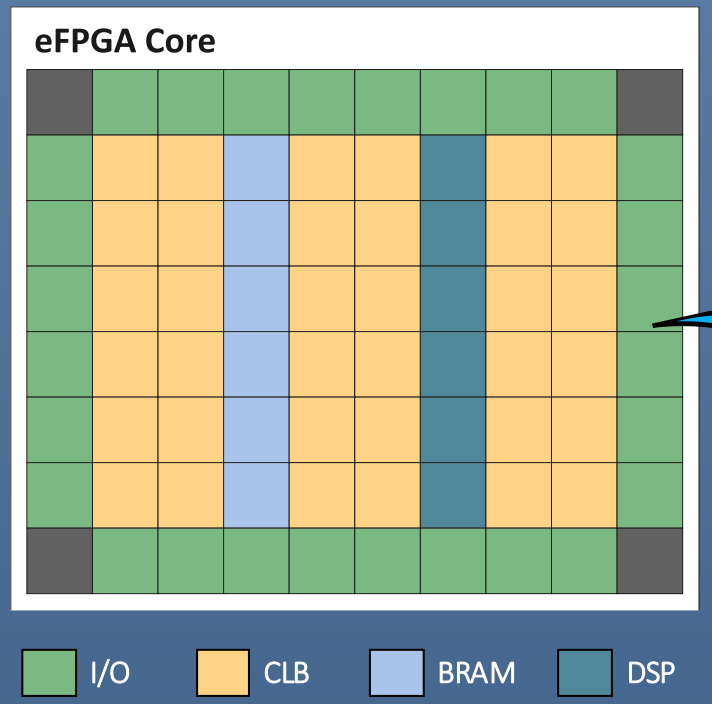


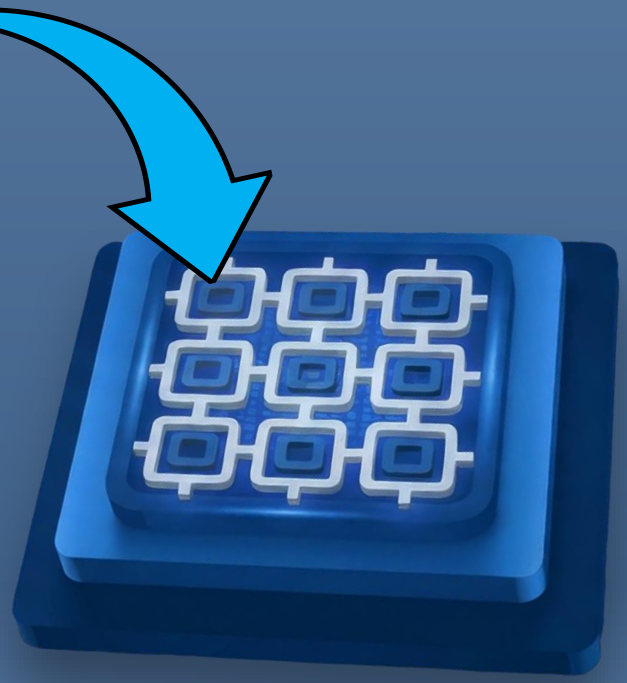
Re-Useable
Common
Chiplets

- Interoperable PHY
- Lowest Power / Cost
- Security
- Management
- Memory
- KGD
- AI
- Sensor fusion

PACE Partner: QuickLogic IP to Chiplet

- **Support Sensor Fusion enabling flexible PHYSICAL AI solutions**
- **Add new features after silicon – no re-spin required**
- **Adapt to changing standards & protocols**
- **Extend product lifetime while reducing risk**

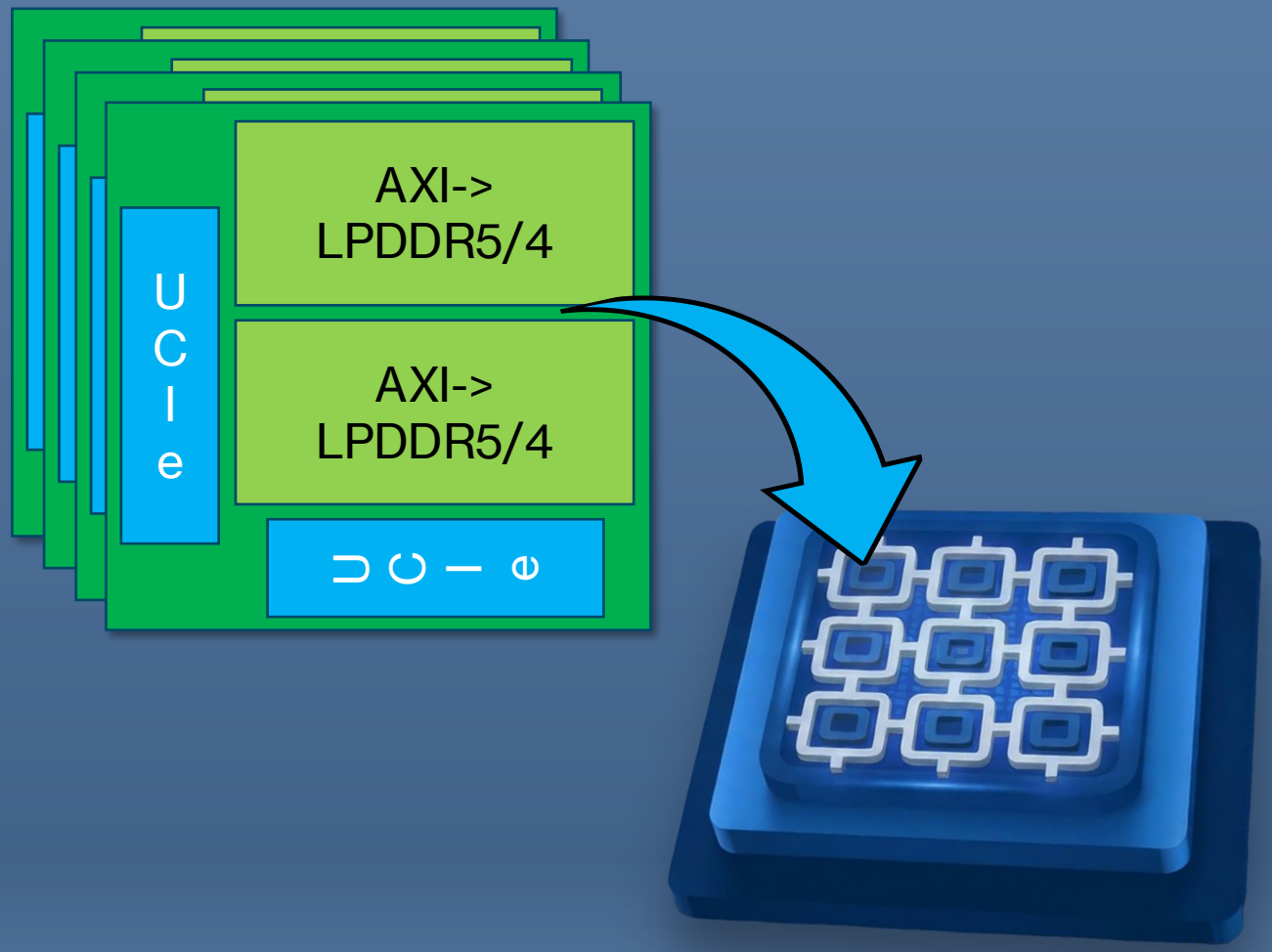




PACE Partner: Breaking Memory Wall

Dolphin Technology

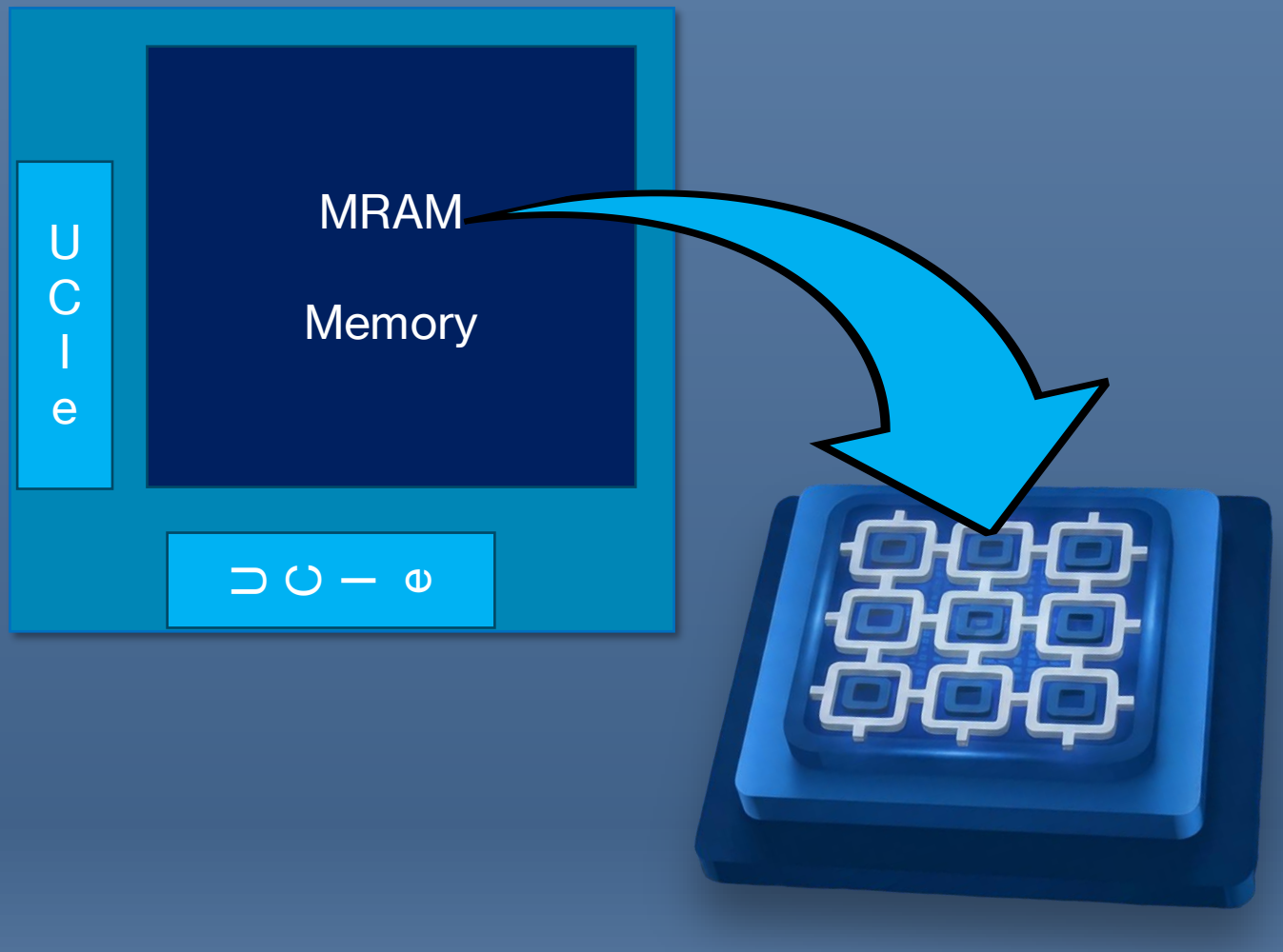
- Silicon Proven LP DDR5/4 PHY IP
- Joint Chiplet with UCIe to AXI to multiple LPDDR banks
- Scalable to massive memory suitable for AI Inference
- Extensible low latency network of LP DDR Chiplets



PACE Partner: high performance NVM

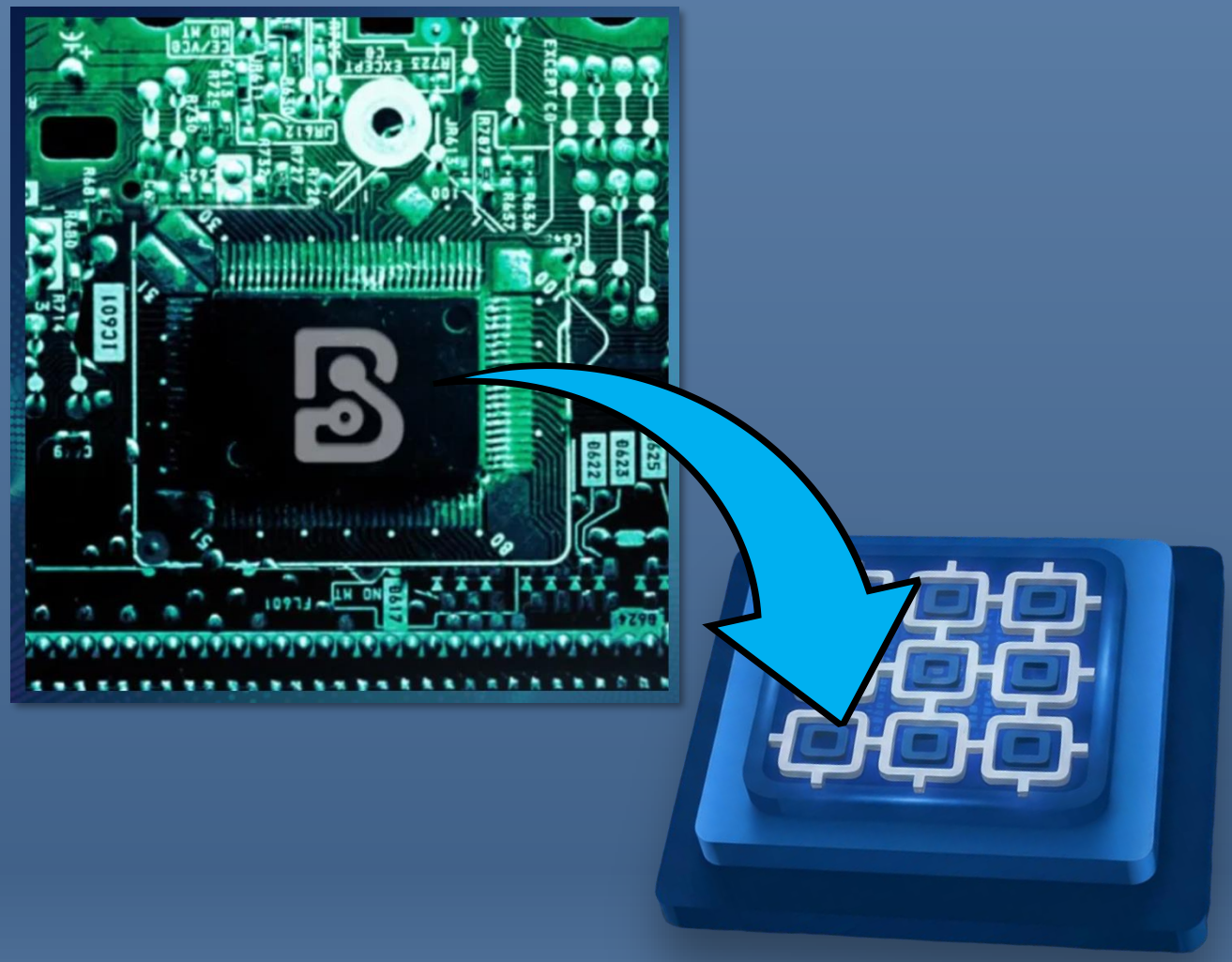
EVERSPIN TECHNOLOGIES

- **High Speed Non-Volatile and robust MRAM memory**
- **Ultra low latency for AI weights**
- **Help store securely Configs**
- **Enable secure boot, ROT and extended FPGA security**



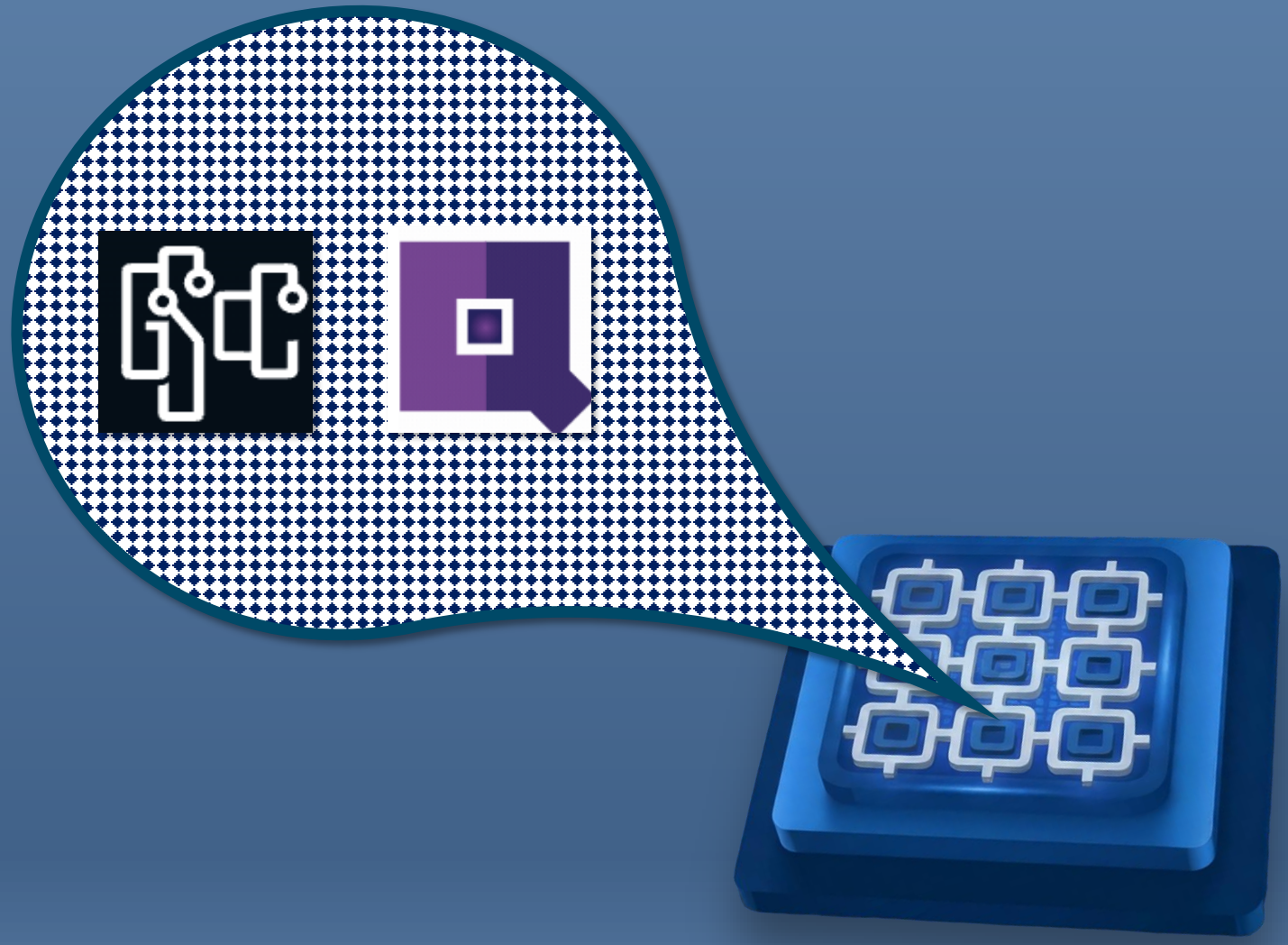
PACE Partner: Blumind – AI Chips & Chiplets

- **Ultra-low power and latency Inference – for Physical AI**
- **Licensable IP & Future Chiplets**
- **Future Chiplets will be based on market demand**
- **All analog design**



PACE Partners: Security and Management Chiplet IP

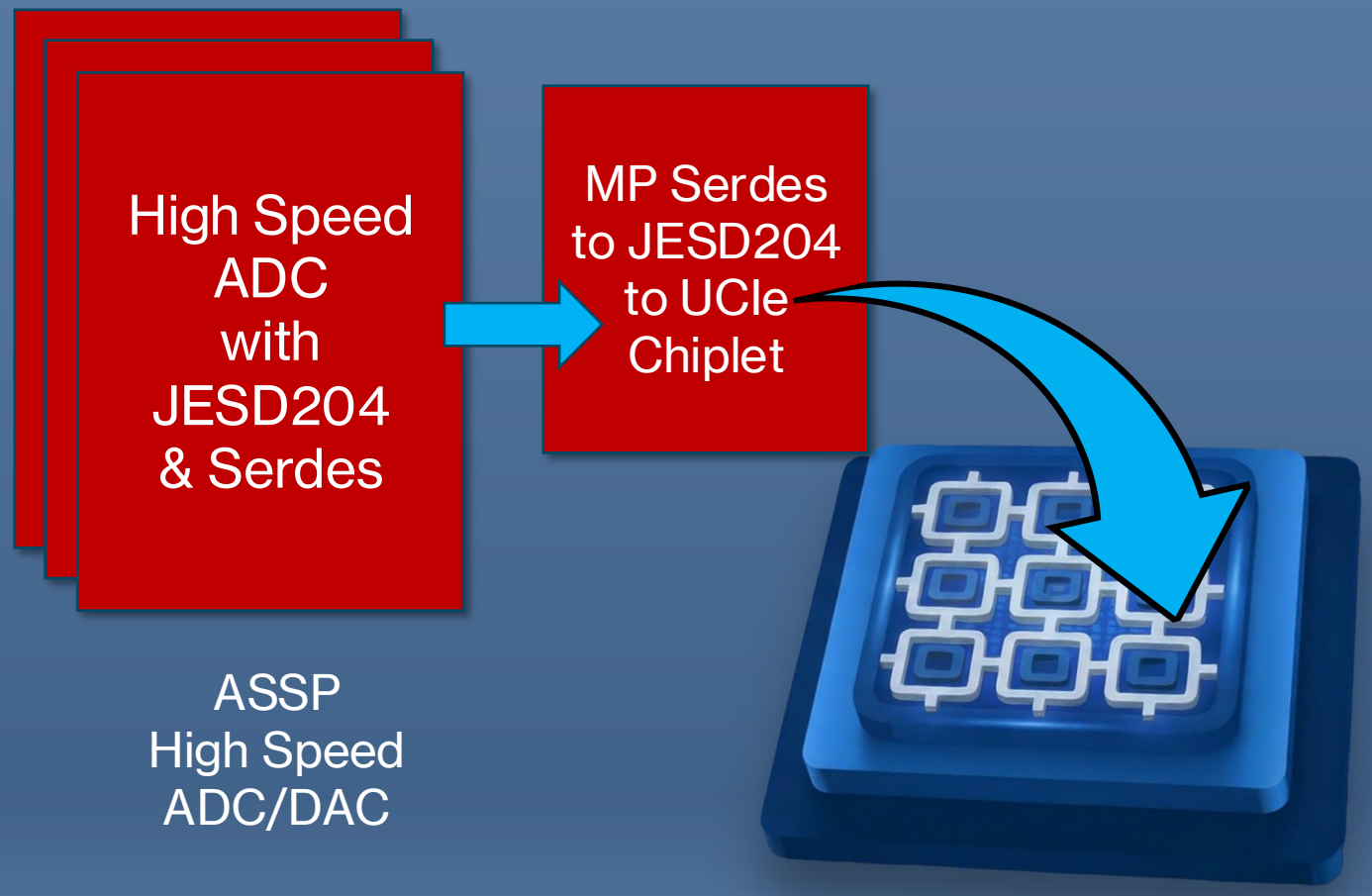
- Root of Trust & PUF for security from Crypto Quantique
- RISC V and Management IP from GSOC
- Secures multiple Chiplets in single chiplet
- System Manager & Lifecycle management



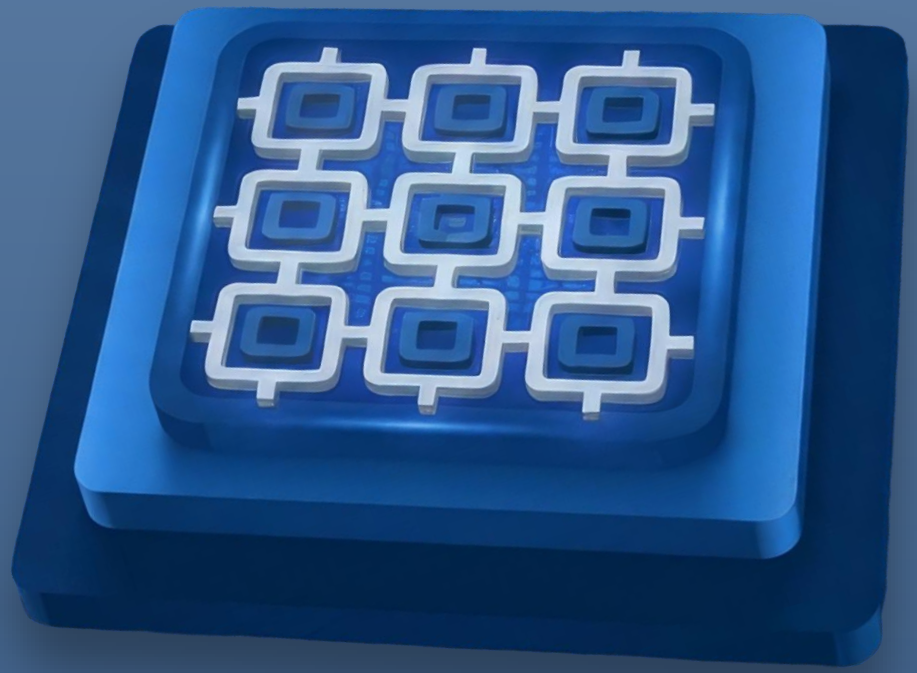
PACE Partners: High Speed I/F IP

Chip Interfaces

- **Leader in JESD 204 over UCIe IP**
- **Expertise in JESD204 over many Serdes IP**
- **Interlaken and Ethernet IP**
- **UCIe controller IP**

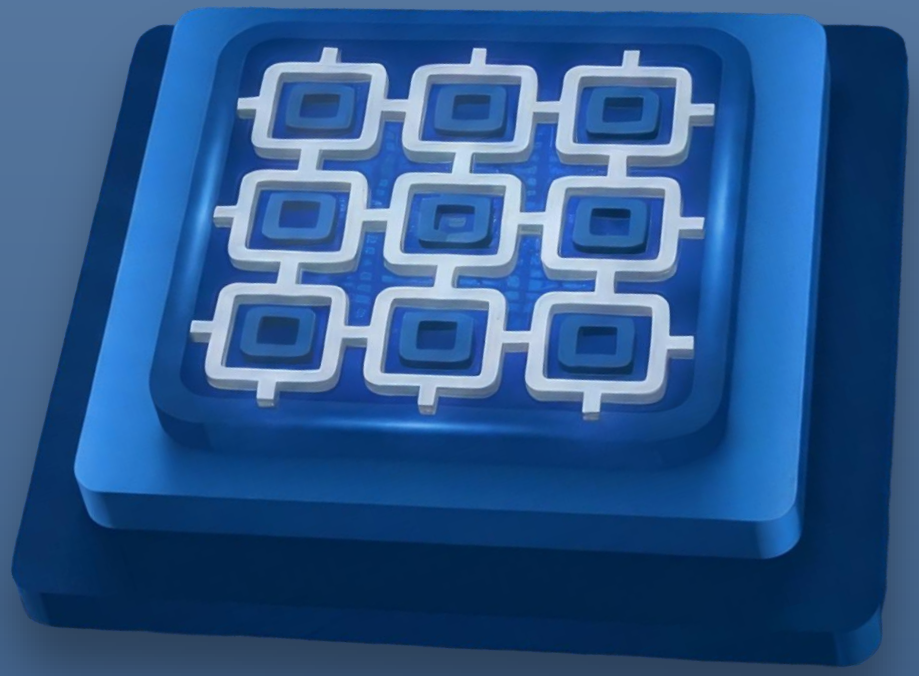


PACE : Breaking the Chiplet Wall



- PACE provides Chiplets & IP
- Faster Time to Market
- Supports Many Foundries
  Nodes 2nm to 28nm +
- Limits Design Risks & NRE
- **Develop your own Chiplet**
  No MPW PHY costs (at 28nm)

PACE : Your own Custom Chiplet



- **Design ASAP - TTM**
- **Pace helps - Free use of PHY**
- **Pace supplies – external PACE re-useable Chiplets**
- **Got to production ASAP**
- **Total NRE Cost savings from $10M+ down to $1M range**


Interested in
Co-developing
Chiplets
Learn more :
info@PaceChiplets.com